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Title of Invention: Low-power bus interface

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REPLY BRIEF

Sir:

Applicant responds to new points of argument raised in the Examiner's Answer of 03/31/2008, as follows.

REMARKS

As acknowledged in the Examiner's Answer of 03/31/2007, the focus of the prior art rejection based on Mitchell has shifted from Fig. 3 of Mitchell to Fig. 1 of Mitchell. In either case, Mitchell fails to teach or suggest important features of the present invention, as described more fully below.

CLAIMS 1-8

An important feature of claim 1 is that an activity detector detects "an initiation of a data-transfer operation ... to provide therefrom an enabling signal that is communicated to bus interfaces of a plurality of ... components, wherein the bus interface is configured to be enabled to receive data from the bus structure *as part of said data-transfer operation* based on receipt of the enabling signal from the activity detector."

That is, from the time the activity detector detects initiation of the data transfer operation, the bus interface is enabled in time to receive data as part of the data transfer operation. Mitchell does not teach or suggest operation in this fashion.

Firstly, it is questionable whether the activity monitor 21 of Mitchell "detects initiation of a data-transfer operation." The power management state (DOZE, SLEEP, SUSPEND, etc.) in Mitchell is set by software running on the CPU. The desired power management state is communicated to the power management unit through the system bus, in particular the address bus and control bus, *not the data bus, which is conspicuously not illustrated.* Whether the transfer of such desired state information itself may be regarded as a data transfer operation is doubtful.

Nevertheless, clearly, Mitchell does not in response enable a bus interface in time to receive data *as part of the data transfer operation.* Whatever data transfer may be said to occur during communication of the desired power management state from the CPU to the power management unit (PMU) in Mitchell, other components in the system do not participate in that data transfer.

Accordingly, Mitchell does not anticipate or render obvious the invention of claim 1.

Claim 2 further recites that the activity detector detects a completion of the data-transfer operation of claim 1. No such statement can be made about Mitchell and its dubious "data-transfer operation."

Claims 5 and 6 further recite that the activity detector includes a set-reset device and a delay device, and that the set-reset device is reset upon detector of a completion of the data-transfer operation. Again, no such statement can be made about Mitchell and its dubious "data-transfer operation."

CLAIMS 10-13

The same distinction drawn with respect to claim 1 applies with equal force to claim 10. That is, Mitchell does not detect initiation of a data-transfer operation and in response enable a bus interface in time to receive data *as part of the data transfer operation.*

Claim11 further recites detecting a completion of the data-transfer operation of claim 10 and disabling the bus interface at more than one component based on the completion of the bus activity. No such statement can be made about Mitchell and its dubious "data-transfer operation."

CLAIMS 15-19

Claim 15 is even more explicit than the claims discussed previously. It recites:

An electronic circuit comprising: a plurality of initiators that are configured to selectively initiate data-transfer operations via a bus structure, an activity detector that is configured to detect an initiation of a data-transfer operation from any of the plurality of initiators, and to generate therefrom an enabling signal, and a plurality of targets that are configured *to process the data-transfer operations*, each of the plurality of targets including an interface for receiving the data-transfer operations, wherein the interface of each of the plurality of targets is configured to receive data of the data-transfer operations in dependence upon the enabling signal from the activity detector.

Mitchell does not detect initiation of a data-transfer operation and in response enable interfaces of targets in time to receive data and *process the data transfer operation.*

Claim18 further recites detecting a completion of the data-transfer operation of claim 15 and disabling the bus interface at more than one component based on the completion of the bus activity. No such statement can be made about Mitchell and its dubious "data-transfer operation."

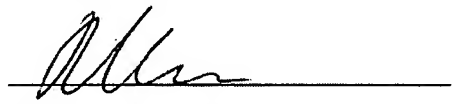
CONCLUSION

In Mitchell, a CPU communicates with a PMU (using address and control lines of a system bus) to place a system in a desired power management state. The clock rate of the system bus is controlled in accordance with the power management state. In the case of a transition from a lower power state to a higher power state, the system bus clock may go from being inactive to being active. Communication with various bus-connected devices may go from being impossible in the old power management state to possible in the new power management state. One may say that a data transfer operation has been enabled.

In Mitchell, however, there is no connection between the detected activity (power management command) and a *possible* subsequent data transfer operation.

In the present invention, by contrast, it is *initiation* of a data transfer operation that is detected and results in device enablement so that *the same data transfer operation* may proceed to completion. This conspicuous difference is reflected clearly in each of independent claims 1, 10 and 15. This same difference is reinforced in various of the dependent claims as discussed above. All of the claims are therefore believed not to be anticipated by, and to patentably define over, Mitchell.

Respectfully submitted,



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